SINGLE PHASE CURRENT-SOURCE ACTIVE RECTIFIER FOR TRACTION: CONTROL SYSTEM DESIGN AND PRACTICAL PROBLEMS

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Summary This research has been motivated by industrial demand for single phase current-source active rectifier dedicated for reconstruction of older types of dc machine locomotives. This paper presents converters control structure design and simulations. The proposed converter control is based on the mathematical model and due to possible interaction with railway signaling and required low switching frequency employs synchronous PWM. The simulation results are verified by experimental tests performed on designed laboratory prototype of power of 7kVA.

1. INTRODUCTION

This research has been motivated by industrial demand for design of single phase current-source active rectifier (CSAR) dedicated for reconstruction of older types of dc machine locomotives. Converter must be able to operate on both trolley voltages: 25kV/50 Hz and 15kV/16 ⅔ Hz. The goal of our research is the realization of the low power (7 kVA) laboratory prototype of this converter.

Development was divided into three stages: control structure simulation, rectifier building and its actuating. Partition of this paper was made in two ways – control structure simulation and control structure actuating. Applied rectifier's control structure is based upon the mathematical model derived from vector diagram (Fig. *1*) and is described in the paragraph 2. The main goal of this paper is to show and describe practical problems which appeared during control structure actuating.

Topic of CSAR is not very common and the published papers mostly deal with the three phase version. Publications are rather theoretical, researches go into the problems connected with control in particular using hysteresis control or PWM modulation (e.g. [1] - [3]). Unfortunately, we did not find any complex paper dealing with single phase version for traction applications.

2. RECTIFIER'S CONTROL POSSIBILITIES AND SIMULATIONS

Function of rectifier's control is to maintain grid (trolley) current curve (i) in harmonic shape and in phase with power grid voltage (u). We can generally use two control methods: hysteresis current control method (for the current consumed from the power grid), or the method using PWM modulation with constant switching frequency. The second method (PWM) is used in the design of CSAR model dedicated for laboratory measurement. This method has been chosen regarding possible interaction with railway signaling, because disturbance produced by constant switching frequency is much easier to eliminate than in case of hysteresis control. Moreover, the PWM control makes possible to employ shifted carriers, which is eligible for high power systems with low switching frequency. In consequence of considered low switching frequency, the synchronous PWM has been implemented.

The power circuit configuration and vector diagram of designed CSAR is shown in Fig. 1. The proposed converter control is displayed in Fig. 2. This structure includes current control loop which independently on phase shift between power grid voltage (U) and grid current ($I_{(1)}$) ensures demanded load current (I_d). The output of load current controller is demanded grid current amplitude ($I_{vm}*$). Cos φ = 1 (zero phase shift between U and $I_{(1)}$) is being reached by control of both angle θ and the amplitude of $I_{V(1)}$. Control of angle θ is based upon the mathematical model derived from vector diagram (see Fig. 1) and is evaluated from known parameters. Its value also has to satisfy the value of required I_d.
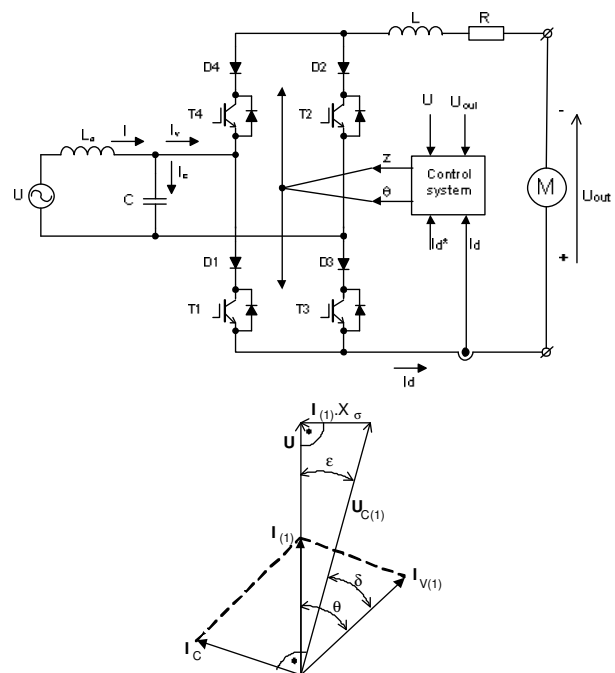

Fig. 1. Power circuit configuration (simulation wiring) and vector diagram for $\varphi=0$
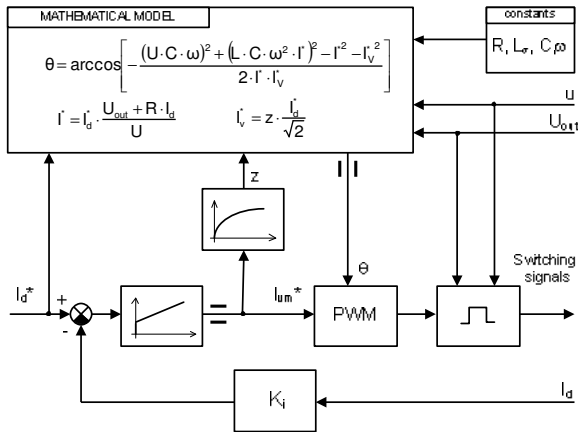
Fig. 2. Designed CSAR control circuit

If the load current is sufficiently high, the designed control works properly and ensures both the required load current and the phase shift φ=0. However, if demanded load current is lower than certain level (I_{dmin}), the control is not able to ensure the zero phase shift (φ=0) between power grid voltage and grid current. When φ=0, the lowest possible $I_{V(1)}$ current value is $I_{V(1)min}=I_{C(1)}$. Therefore, the minimum I_{dmin} is determined by $I_{v(1)min}$. In this case, the converter control structure controls only I_d current value by means of duty cycle (z), while angle θ is permanently set to zero. This solution was derived from the principle of control structure and the fact that with θ = 0, the load current ripple is minimal. This result has been confirmed by simulations. In this case angle φ is not controlled and depends only on the load parameters.

The solution for the above described problem with controllability of θ (and of course φ) is to choose the lowest possible capacitance of the input filter capacitor (C). On the other hand, the capacitance must also satisfy the condition of acceptable u_C voltage ripple and must respect the required filter resonant frequency.

From this is evident big disadvantage of this model-based control structure (Fig. 2), which requires knowledge of R, Lσ, C and ω (power grid frequency). The control requires measurement of I_d, U, U_{out}. Duty cycle (z) is being derived from the load current controller output (I_{vm}^*) by means of low-pass filter. Supply voltage (power grid voltage) measurement is also important due to time synchronization of control algorithm with this voltage and power components switching logic.

Simulations were made in programming language PASCAL with the main emphases on the control principle verification. It was made with respect of serial diodes reverse parameters, switching components (IGBTs) were considered ideal. Examples of simulation results are shown on Fig. 3 - Fig. 5.

It is clear that it is necessary to beware to the input filter (LσC) resonant frequency. Switching (carrier) frequency chosen near this resonant frequency causes vibration of this circuit. To reach the minimal distortion of grid current the smoothing inductor (L)

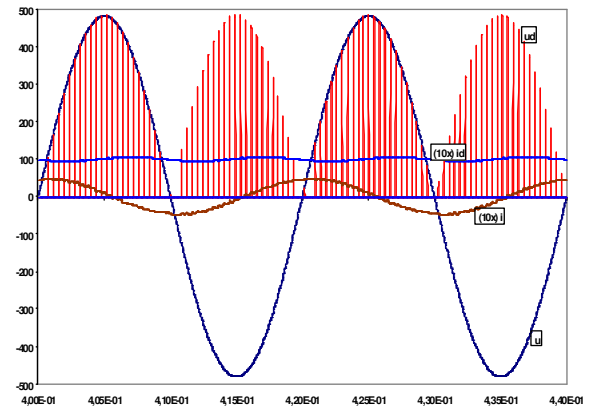should be approximately 3 times higher then in common rectifier.

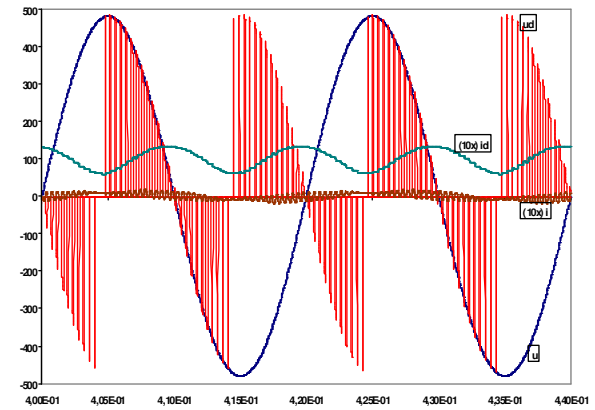*Fig. 3. Simulation result: Id* < Idmin (controlled only duty cycle z, θ = 0)*

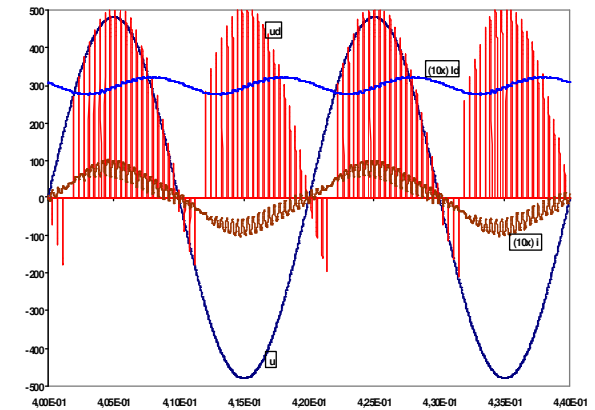*Fig. 4. Simulation result: Id* > Idmin , close to Idmin*

Fig. 5. Simulation result: 4c Id* > Idmin

3. SYNCHRONIZATION PROBLEMS

In order to keep proper function of CSAR, it is necessary to synchronize the control structure with power grid voltage curve. Modulation curve frequency must be coincidental with power grid frequency with respect of voltage polarity. This information can be obtained by different ways depending on how much information we have to know about the voltage curve. When supposing

purely sinusoidal voltage curve, we do not need to observe its shape. In this case we only need to know the moments when the voltage curve crosses the zero axes (moments of polarity change) and the voltage polarity in every half-period. The easiest way to follow this condition (which is also used in our application), is to convert sinusoidal curve (power grid voltage) into the square shape with logical levels of 0 and 3V, otherwise log. 0 and log.1 as well. Log. 0 corresponds to negative half-wave, log. 1 to positive. Signal edges indicate the zero crossings.
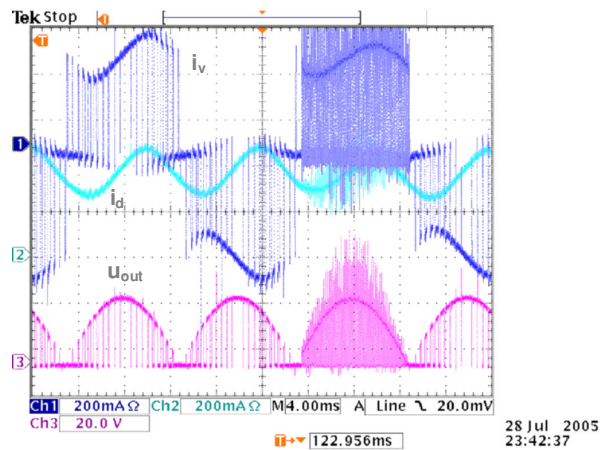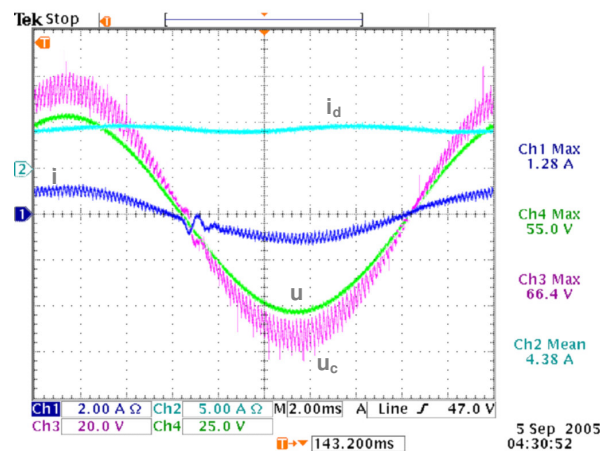

Fig. 6. Failure state of period measuring

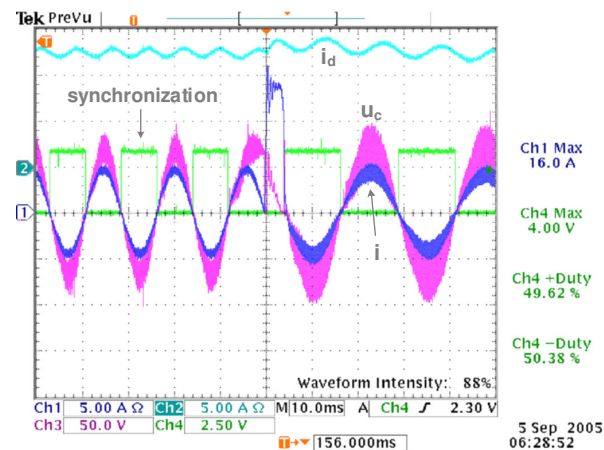*Fig. 7. Grid current resonant glimmer*

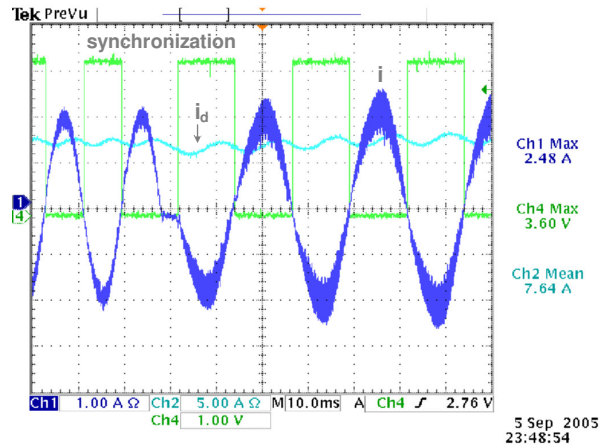*Fig. 8. Faulty response to grid frequency step change*

Fig. 9. Zero vector insertion – proper response to grid frequency step change
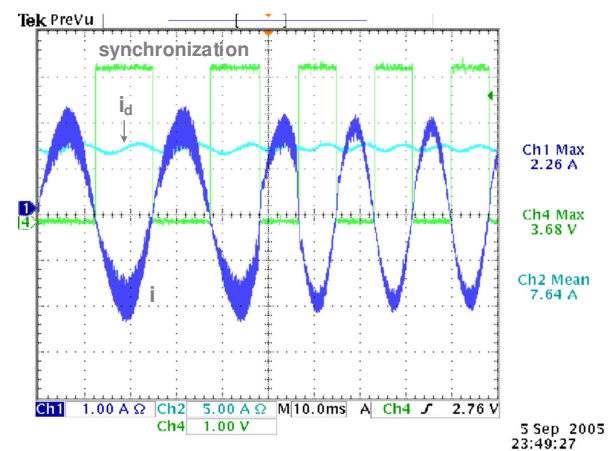

Fig. 10. Proper response to grid frequency step change: increased frequency

Processor evaluates these zero crossings by means of external interrupt; polarity is evaluated from the zero crossing direction - rising or falling edge.

This easy principle approved itself during testing despite a few limitations. Sinusoidal / square converter is realized outside the DSP, where voltage transducer signal disturbance appeared due to power transistors switching. Converter evaluated these glimmers like a multiple polarity change, which also caused the glimmers of square synchronization edges. Frequency measuring has been realized by time measuring between two following edges and this time was consequently used for following half-period. Because of glimmers in synchronization, processor evaluated the time between two following glimmers like a half-period time followed by fault state which caused high switching frequency during the following half-period of about 20 kHz (*Fig. 6*) – the switching frequency increased due to employed synchronous PWM.

The solution of this problem was software implementation of glimmers insensibility. Its principle is to accept only the first coming edge and ignoring the rest during the preset time that is of course shorter than the time of longer half-period to be expected. Another valid edge is the following zero crossing.
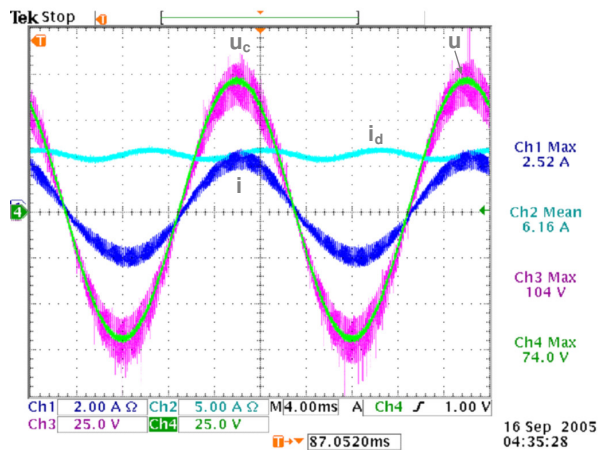
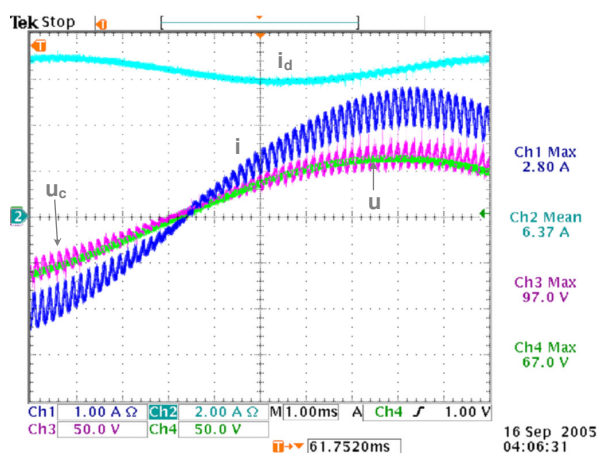*Fig. 11. Final CSAR prototype: Id, I, U a UC in steady state*

Fig. 12. Detail of waveforms from Fig. 11

Another complication of this synchronization method is the duty cycle accuracy. As already mentioned, DSP measured the first voltage half-period time which was then used for setting of following half-period modulation curve. This way has an advantage in faster response on frequency change, but has also greater demand on duty cycle accuracy. If the first half-period is shorter than the following one, in the second half-period the modulation curve comes into zero earlier then voltage curve and a gap in the grid current appear. If the situation is opposite, which means the first half-period is longer then the following one, the overlay of modulating curve over the real one happen. When the polarity of grid current during switching-over is not in zero yet, resonant glimmer of grid current appeared and frequency of glimmers is given by input LC filter. This situation is shown in Fig. 7. The solution was to alternate between measuring of the first half-period and the following one and set the modulation curve period according to these alternating values. This way eliminated grid current glimmers during zero crossing.

Another problem appeared during power grid voltage frequency step change (Fig. 8). After faulty reaction of half-period length change early switch-over of switching transistors for positive and negative power grid voltage half-period. Consequently, the

CSAR carried on like a diode rectifier which means that grid current increased rapidly and was given only by load parameters. As a precaution of this fault we gained zero vector inserting (realized as a load short circuit). If the modulation curve crosses zero axes earlier then power grid voltage, zero vector continues until the next edge indicating next voltage zero crossing occur (Fig. 9). This precaution has one more function, because when outage of power grid happen (e.g. trolley bounce), load current I_d decreases continuously to zero. Opposite situation happen when frequency increases (Fig. 10). Modulation curve can not finish the cycle and switch-over happen with nonzero current i. In this case the control structure is able to avoid the overcurrent shown in Fig. 8.

Fig. 11 and Fig. 12 confirm the proper behaviour of the final prototype employing all above described improvements of both control system and power circuit.

4. CONCLUSION

The designed laboratory prototype (7kVA) of traction CSAR employs model-based control system with synchronous PWM. This method has been chosen regarding possible interaction with railway signaling, because disturbance produced by constant switching frequency (especially in case of synchronous modulation) is much easier to predict and, therefore, eliminate than in case of hysteresis control. Moreover, the PWM control makes possible to employ shifted carriers, which is eligible for high power systems with low switching frequency. The simulation and experimental results confirm proper function of designed control structure under both steady state and transient conditions. The experiments also verified the correct converter behaviour during the faults. The biggest disadvantage of proposed model-based control is necessity of input filter parameters knowledge and the reduced robustness against parameter variations. The actual research is focused on the improvement of converter behaviour under distorted power grid voltage.

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